

(SYLLABUS)

1.

(Course Title)	Project	(Instructor)			
(Year)	2026	(Semester)	2	(Course No.)	2150084801
(Class)	01	(Open to)	3, 4	(Course Classification)	-
/	3.0 / 03 / 3		100	가	가
(Office)		(Telephone)	02-828-7489	(e-mail)	inchul.song@ssu.ac.kr
	(PBL)				
	(*) (ABEEK Classification)		(*) (ABEEK Requirement)		
	: (Verilog-HDL, C) : , FPGA				
(Course Description)					

SoC AI HW IP	
SoC platform (CPU, bus architecture, memory system) AI HW IP	
SoC platform AI HW IP SW (Platform SW, SW IP)	

가	(100)	(100%)
	20	20
	20	20
	40	40
	20	20

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(Required Texts)		* /SoC AI HW IP / /
	()	
	FPGA SW AI	
	1) : (+)20%, 20%, Project 40%, 20%. 2) (> Sys.LSI > Modem Engineer): ASIC 가 1 , SoC 가 1 , Embedded SW 가 1 1 .	

2.

(Week)	(Keyword)	(Description)		(Texts)
01		CMP Project , CMP Proejct (3 1)		
02	(1)	SoC Architecture, SoC subsystem, SoC component SW interface HW accelerator		
03	(2)	ASIC vs. FPGA, Verilog-HDL coding guide, Sanity check (Lint, CDC, Memory access rule, Synthesis log), Function coverage & code coverage		
04	(3)	SW Embedded SW Embedded SW coding guide, HW IP SW		
05		(CMP) CMP project feedback, (CMP) HW feedback		
06	FPGA HW	FPGA Board , FPGA vs. HDL design flow (PL & PS) , PL(Programmable Logic) HDMI Monitor		
07	SoC SW	SoC CPU/AMBA bus/HW IP , Platform SW/SW IP/driver SW PS(Processing System) HDMI Monitor		
08	Partitioning HW	HW/SW (1/2), HW , PL Camera		
09	Partitioning SW	HW/SW (2/2), SW , PS Camera		
10	Project (1/4)	(CMP) Project , project specification (1/4) (CMP) Conv. , project specification , (1/4)		
11	Project (2/4)	SW Conv. , SW contorl (2/4)		

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12	Project (3/4)	Project Q&A, (3/4)	, , , ,	
13	Project (4/4)	feedback (4/4)	, , , ,	
14	Project	Project	, ,	
15		()		

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3. ()

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	Open-ended problem		
	Teamwork		
	Communication skills		